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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,027	11/21/2001	Nobuo Yamasaki	216349US2	9844

22850 7590 11/30/2005

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EXAMINER	
DHARIA, PRABODH M	
ART UNIT	**PAPER NUMBER**
2673	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,027	YAMASAKI, NOBUO	
	Examiner	Art Unit	
	Prabodh M. Dharia	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-27* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-21-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. **Status:** Receipt is acknowledged of papers submitted on 01-28--2005 under request for reconsideration have been placed of record in the file. Claims 1-27 are pending in this action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,636,194 to Ishii in view of US Patent 6,522,319 to Yamazaki and Sato et al.(5,712,652).

In reference to claims 1, 7, 10, 11, 12, and 17, Ishii teaches an invention that is similar to the one being claimed. Figures 1 and 2 shows several critical components of Ishii's invention that anticipates the claimed invention. As shown in the figures, Ishii teaches a plurality of data lines and scan lines (115 and 110 respectively) and a plurality of pixels disposed at their intersection (item 105). Ishii's invention also includes a plurality of pixel switching element that conduct the data line information according to the scan (item 109). Ishii includes data driver (114) and scan driver (201) for controlling the write of the graphic data. The crux of the similarity behind the two inventions lies in memory device driver (item 102) and power source voltage control circuit (item 104). The memory device driver (102) controls the write of the data held in memory when the display switch is in (column 6, lines 14-25) second display mode. The power source voltage

control circuit (104) is used for stopping the power source voltage during the second display (column 6, lines 25-30).

The difference that lines between Ishii's invention and the claimed invention is most apparent in the power source voltage generation and control.

Ishii teaches switching the conduction modes from on to off, but does not teach suspending the generation of the actual power source. As one skilled in the art understands, scan and data circuits inherently must be power. Therefore, the inventions deviate not on whether the circuits should be powered but how the power is controlled.

Yamazaki teaches an invention similar to Ishii's. Yamazaki teaches a LCD that achieves power conservation through a hold mode display period. Yamazaki teaches on column 7, lines 34-43 that the voltage source is suspended during the second display mode to achieve better power conservation.

Ishii's invention can be modified to resemble the claimed invention by adding Yamazaki's power source. In fact Yamazaki, on column 16, line 3 teaches that pixel with memory displays (much like the one discussed in Ishii) are highly applicable to this power saving scheme. It would have been obvious to include Yamazaki's power source into lshii's invention in order to achieve more efficient power conservation, suspending power expenditure during times where new data does not need to be supplied to the pixels.

Ishii teaches switching the conduction modes from on to off, but does not teach suspending the generation of the actual power source. As one skilled in the art understands, scan and data circuits inherently must be power. Therefore, the inventions deviate not on whether the circuits should be powered but how the power is controlled.

Sato et al. teaches discloses the digital memory cell holds the preceding video signal until the new succeeding video signal is written, image can be kept displayed as a still image and scan line and data line signals are stopped. (Col. 3, lines 66,67, Col. 4,lines 1-7, Lines 36-57,Col. 13,Lines 8-33).

Ishii's invention can be modified to resemble the claimed invention by adding Sato et al. teaching. It would have been obvious to include Sato et al. teaching into lshii's invention in order to achieve more efficient power conservation, suspending power expenditure during times where new data does not need to be supplied to the pixels.

In reference to claim 2-5, it can be seen from figure 15 that the power source is connected to both the scan and data drivers and switches off during "the period of partial display state" (column 7, line 37).

In reference to claims 6 and 16, it is Yamazaki teaches a DC/DC converter, more specifically a charge pump.

In reference to claims 8, 9, 18 and 19, it can be seen from figure 2 of Ishii-that the pixel memory implemented by Ishii is SRAM with inverts 103-1 and 103-1 with a switch 102.

In reference to claim 14, Yamazaki in figure 2 teaches a power source generator that includes boosting units (9, 10) and output smoothing capacitors. In figure 5, Yamazaki discloses the details of the control circuit where a comparator is used to determine the charge pump operations.

In reference to claim 15, controlling circuit includes an AND circuit that receives the comparison results (15) and mode switching signal. The AND circuit serves as a stop for the comparison signal to the boosting unit.

In reference to claims 20-22 and 24-26, column 6, lines 14-23 Ishii teaches the two modes where in memory mode, data is nonconducting and the information is supplied from the memory circuit. As explains in column 3, lines 5-12 since there is no need to rewrite screen display the display state is held by the memory circuit (still image display mode).
In reference to claims 23 and 27, as one skilled in the art understands the memory circuit proposed by both Ishii and the applicant is only capable of binary information. Therefore such a limitation is inherent to the design of the display circuit.

Response to Arguments

4. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

5. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an examiner's statement of reasons for allowance:

A display device comprising: a memory device-built-in pixel portion including a plurality of data lines and a plurality of scan lines arranged in a matrix, a plurality of pixels disposed on respective intersections of the both lines, a plurality of pixel switching elements electrically conducting the data lines and the pixels based on scan signals supplied to the scan lines to write graphic data supplied to the data lines into the pixels, and a plurality of memory devices storing the graphic data supplied to the data lines and being constituted to be capable of supplying the graphic data stored to the pixels corresponding thereto; a data driver and a scan driver for controlling the write of the graphic data supplied to the data lines into the pixels in order to perform a first display; a memory device driver for controlling the write of the graphic data held in the memory devices into the pixels in order to perform a second display; a power source voltage generating unit for supplying a power source voltage to the data driver and the scan driver; and **a power source voltage generating and stopping circuit for stopping generation of the power source voltage in the power source voltage generating unit during a period of the second display.; wherein the power source voltage generating unit includes a switching boosting unit for boosting an input voltage, an output smoothing unit for smoothing the voltage boosted in the switching boosting unit to set the voltage as an output voltage, a comparator for controlling a boosting operation of the switching boosting unit in response to a comparison result of the output voltage with a reference voltage, and a power source voltage generating and stopping circuit connected between the comparator and the switching boosting unit, and the power source voltage generating and stopping circuit stops**

the boosting operation in the switching boosting unit by electrically disconnecting the switching boosting unit and the comparator during the period of the second display.

Cited references on 892's fails to teach underlined bold claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shintani et al. (5,875,034) Camera system ahving recordable medium positioned between photographing and reproducing portions.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

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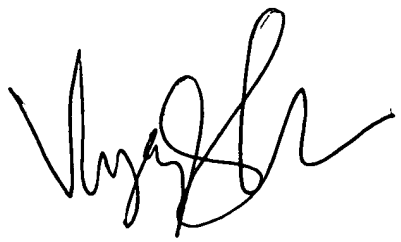
November 21, 2005



VIJAY SHANKAR
PRIMARY EXAMINER